**Course Syllabus**

**Computer Architecture, ELL305 (3-0-0)**

Tue/Wed/Fri 10am-11am

**LH 114**

Autumn 2024

(**Course Coordinator**)

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**Office Hours:** Wednesday, 5:00-6:00 pm

**TENTATIVE COURSE SCHEDULE:**

**TKG** [Introduction to Computer Architecture, Fundamentals of computer Design, Number systems, Logic gates, registers, memory, Language of bits, assembly language, Computer arithmetic, Performance measurement, Instruction Set Architecture].

**SDR** [Processor: ALU/CPU design, Control design (GCD Divisor, GCD multiplier), Finite State Machine (FSM), Control design, ARM, Assembly Language, Data Path, Pipelining, Memory system; Hierarchy, Memory Technology, Main memory, Virtual Memory, High Speed memories, Memory management]

**SK** [Multicores, Multiprocessors, Clusters, GPU, I/O management and Networking, Pipelining]

**Grading criteria:**

Minor : 33 marks (3 marks quizzes+30 marks)

Additional Minor : 33 marks (3 marks quizzes+30 marks)

Major: 34 marks (4 marks quizzes+30 marks)

1-1.5 Hours exam after each Instructor’s Class (Preferably in Weekends)

**Textbook:**

J. L. Hennessey, D. A. Patterson. *Computer Architecture: A Quantitative Approach.* Fifth Edition, Elsevier, 2012.

**Reference Books:**

* D. A. Patterson, J. L. Hennessey. *Computer Organization and Design: The Hardware/Software Interface.* Third Edition, Elsevier, 2005.
* S.R. Sarangi. Computer Organization and Architecture
* J. P. Hayes. *Computer Architecture and Organization.* Third Edition, WCB/McGraw-Hill, 1998.
* K. Hwang, F. A. Briggs. *Computer Architecture and Parallel Processing.* McGraw-Hill, 1985.